Hybrid Analysis of Large Interconnects and Nonlinear Circuit Using Hierarchical Technique

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Abstract

This paper describes a hybrid analysis of large interconnects and nonlinear circuits using the hierarchical technique and the fast simulation technique. First, we introduce the typical linear circuit formulation. Next, we describe the way to derive the macromodel of the linear circuit and apply it to the hierarchical formulation of the whole circuit. Then, the simulation algorithm is shown. Moreover, a computational complexity of the proposed technique is also described.

1. Introduction

As the high-speed and high-density electronic circuit design of the latest LSIs progresses, various effects which depend on the high-frequency characteristics of the signals are induced on the chips and packages. Because these effects cause the uncomfortable behaviors of the chips and packages on a printed circuit board, it becomes important to verify the electronic circuit behaviors including these effects. From a circuit simulation point of view, a net-list, which is mainly provided by an extractor that extracts circuit element parameters from the object to be analyzed and outputs them as the net-lists, includes an enormous number of parasitic elements in order to verify the exact behaviors of the chips and packages. In addition, switching devices such as MOSFETs which have nonlinear behaviors have to be simulated with those parasitics. These facts cause the large amount of simulation time for a SPICE-like simulator based on the matrix solver. Therefore, a fast simulation method which is different from SPICE-like ones is strongly demanded. Our recent researches indicate that Latency Insertion Method (LIM) in [2] and the relaxation-based method in [4] could be one of the noticeable methods for the fast simulation of large linear networks. Because the methods described in [2] and [4] circumvent matrix operations to solve a circuit equation for the large networks, they can perform a faster simulation than conventional ones.

In this paper, we propose one of the techniques for a hybrid analysis of large interconnects and nonlinear circuits using the hierarchical technique and the fast simulation technique. The hierarchical technique is proposed in [1] for an efficient power distribution network (PDN) simulation in terms of the computational time and required memory. In general, however, a nonlinear circuit is assumed to be separated from PDN, which becomes a very large linear circuit, in the simulation: It is true that currents moving from the nonlinear circuit to the linear networks are considered, but each circuit area is analyzed completely individually with the assumption that the feature of the other area is ignored. Since they connect to each other originally, however, it is natural and often needed to simulate them together as a hybrid system of the linear and nonlinear circuits. The SPICE-like simulators solve the hybrid system in a lump by a direct method, and therefore, the simulation becomes intractable immediately as the number of the circuit elements increases. On the other hand, our technique can analyze separately the linear and nonlinear parts of the hybrid system using the hierarchical technique as well as include the interactive effects between the linear and nonlinear circuits. Once a circuit is separated, we can apply the fast transient analysis technique such as LIM and the relaxation-based method to the large linear circuit simulation. And therefore, computational costs are effectively reduced in the simulation as a whole.

First, we introduce formulation techniques for a linear circuit. Next, we describe the way to derive the macromodel of the linear circuit and apply it to the hierarchical formulation of the whole circuit. Then, the simulation algorithm for the hybrid analysis of large interconnects and nonlinear circuits using the hierarchical technique and the fast simulation technique is shown. We also describe the computational complexity of the proposed technique and some techniques to reduce it. In conclusions, it is confirmed that the proposed technique can analyze the hybrid system of the large interconnects and the nonlinear circuit adequately and more effectively than conventional ones.

2. Formulation Using Hierarchical Technique

In this section, we propose an application technique of the

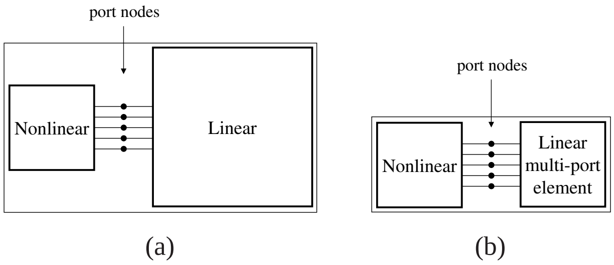


Figure 1: Diagrams of circuit to be analyzed. (a) Large linear circuit part and nonlinear part which are connected each other at several port nodes. (b) Nonlinear circuit with linear multi-port element.

hierarchical technique to the hybrid analysis of large linear networks with nonlinear circuit elements as shown in Fig. 1(a). The hierarchical technique is used efficiently in the hierarchical analysis of PDN [1]. We assume that the circuit to be analyzed is dominated by large linear networks and nonlinear circuit elements exist in relatively small parts of it. In this case, the whole circuit itself is regarded as a nonlinear circuit, and therefore, conventional matrix-based techniques suffer from the calculation cost of a large Jacobian matrix in a transient analysis. This is because the conventional ones formulate a whole circuit in a lump into a large circuit equation with the modified nodal analysis (MNA) method. And the equation results in an ordinary differential equation (ODE) including all voltage and current variables in the circuit. Thus, we have to solve the equation which include a large number of the variables at a time in a conventional way.

In the hierarchical analysis of PDN, the equivalent circuit of PDN is assumed to be composed of a *global* grid and several *local* grids. And then, the global grid is formulated and analysed using the *macromodels* of the local grids. Similarly, the proposed technique regards linear networks as one local grid and derives the macromodel of it primarily. Using the macromodel, because linear networks can be regarded as a linear multi-port element from the view point of the nonlinear circuit, the whole circuit is analyzed by analyzing the nonlinear circuit, corresponding to the global grid, to which the linear multi-port element is connected. First, we describe the way to derive the macromodel of the linear networks, and then, formulate the circuit equation to be solved using the macromodel.

2.1. Formulation for Typical Linear Circuit

In general, a linear circuit which consists of passive linear components such as a resistor, an inductor, a capacitor and independent voltage and current sources can be formulated using the nodal analysis (NA) method with companion models [4] in the matrix form as

$$\mathbf{G}_{\mathrm{L}} \cdot \mathbf{v}_{\mathrm{L}} = \mathbf{b}_{\mathrm{L}}, \tag{1}$$

where $\mathbf{G}_{\mathrm{L}}$ is the admittance matrix, $\mathbf{v}_{\mathrm{L}}$ is the voltage variable vector and $\mathbf{b}_{\mathrm{L}}$ is the current source vector, respectively. In this case, every inductor and capacitor in the circuit is transformed into an equivalent resistance and current source by using a companion model in this formulation, and therefore, the values of the equivalent current sources are changed at each time step. Thus, we should specify the time steps of $\mathbf{v}_{\mathrm{L}}$ and $\mathbf{b}_{\mathrm{L}}$ as $\mathbf{v}_{\mathrm{L}}^{n+1}$ and $\mathbf{b}_{\mathrm{L}}^{n}$, where n is the time step, however, they are dropped for clarity in (1).

In addition, an almost same equation can also be formulated eventually in the form of (1) as follows: First, using the MNA or RLCG-MNA method [3], we can derive the ODE written as

$$\tilde{\mathbf{G}} \cdot \mathbf{x} + \tilde{\mathbf{C}} \cdot \dot{\mathbf{x}} = \tilde{\mathbf{b}}, \tag{2}$$

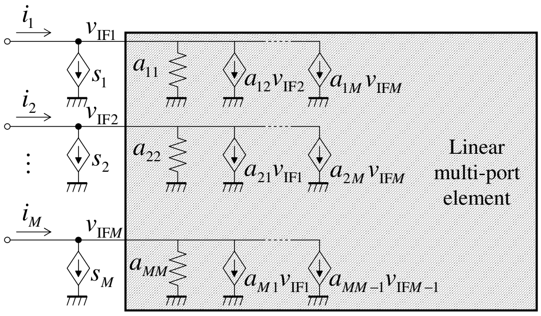
where $\tilde{\mathbf{G}}$ is the conductance matrix dependent on each method, $\tilde{\mathbf{C}}$ is the admittance matrix, $\mathbf{x}$ is the variable vector resulting from voltage and current variables and $\tilde{\mathbf{b}}$ is the independent source vector resulting from current and voltage sources, respectively. Then, applying a numerical integration technique, e.g. the trapezoidal formula, to (2) and transforming the equation lead to

$$\left(\frac{\Delta t}{2}\tilde{\mathbf{G}} + \tilde{\mathbf{C}}\right) \cdot \mathbf{x}^{n+1} = \left(-\frac{\Delta t}{2}\tilde{\mathbf{G}} + \tilde{\mathbf{C}}\right) \cdot \mathbf{x}^{n} + \frac{\Delta t}{2}\left(\tilde{\mathbf{b}}^{n+1} + \tilde{\mathbf{b}}^{n}\right), \tag{3}$$

where n is the time step and Δt is the time step size. It is confirmed that the form of (3) is the same as one of (1) by regarding the coefficient matrix as $\mathbf{G}_{\mathrm{L}}$, the variable vector as $\mathbf{v}_{\mathrm{L}}$ and the right hand side as $\mathbf{b}_{\mathrm{L}}$ at $(n+1)$-th time step. Note that although they have the same form, it seems that the extra current variables are induced if some inductors or voltage sources exist in the circuit; the number of the variable in (3) is larger than that in (1). Moreover, the coefficient matrix in (1) is the positive definite symmetric matrix while one in (3) is not. Eqs. (1) and (3) can be formed at each time step and we can obtain the values of the voltages in the circuit by solving it at each time.

2.2. Macromodeling for Linear Circuit

As mentioned above, the circuit to be analyzed is composed of a linear circuit part and a nonlinear one. We now define the node which is a junction node between two parts as a port node as shown in Fig. 1(a). Thus, both linear and nonlinear circuit elements can be connected to a port node. In order to derive the macromodel of a linear circuit, the nonlinear part which consists of not only nonlinear circuit elements but also linear ones is excluded from the circuit. In other words, considering only the linear circuit part including



(a)

$$\boxed{\mathbf{i} = \mathbf{A}\mathbf{v}_{\mathrm{IF}} + \mathbf{S}}$$

$$\Leftrightarrow \quad \mathbf{A}\mathbf{v}_{\mathrm{IF}} = \mathbf{i} - \mathbf{S}$$

$$\Leftrightarrow \quad \begin{bmatrix} a_{11} & a_{12} & \cdots & a_{1M} \\ a_{21} & a_{22} & \cdots & a_{2M} \\ \vdots & \vdots & \ddots & \vdots \\ a_{M1} & a_{M2} & \cdots & a_{MM} \end{bmatrix} \begin{bmatrix} v_{\mathrm{IF1}} \\ v_{\mathrm{IF2}} \\ \vdots \\ v_{\mathrm{IF}M} \end{bmatrix} = \begin{bmatrix} i_1 \\ i_2 \\ \vdots \\ i_M \end{bmatrix} - \begin{bmatrix} s_1 \\ s_2 \\ \vdots \\ s_M \end{bmatrix}$$

(b)

Figure 2: (a) Circuit topology of a linear multi-port element. (b) Matrix form of (11) using macromodel of linear circuit.

the port nodes and formulating the linear circuit part with the port nodes lead to the equation in the form of (1), for more details,

$$\begin{bmatrix} \mathbf{G}_{\mathrm{L11}} & \mathbf{G}_{\mathrm{L12}} \\ \mathbf{G}_{\mathrm{L12}}^{\mathrm{T}} & \mathbf{G}_{\mathrm{L22}} \end{bmatrix} \begin{bmatrix} \mathbf{u}_{\mathrm{L}} \\ \mathbf{v}_{\mathrm{IF}} \end{bmatrix} = \begin{bmatrix} \mathbf{b}_{\mathrm{L1}} \\ \mathbf{b}_{\mathrm{L2}} + \mathbf{i} \end{bmatrix}, \tag{4}$$

where $\mathbf{u}_{\mathrm{L}}$ and $\mathbf{v}_{\mathrm{IF}}$ are the voltage vectors at the internal nodes in the linear circuit part and the port nodes, respectively. Additionally, $\mathbf{G}_{\mathrm{L11}}$ and $\mathbf{G}_{\mathrm{L22}}$ are the admittance matrices of the internal and port nodes, $\mathbf{G}_{\mathrm{L12}}$ is the admittance matrix resulting from the associations between the internal nodes and the port nodes, and $\mathbf{b}_{\mathrm{L1}}$ and $\mathbf{b}_{\mathrm{L2}}$ are the vectors of current sources connected at the internal and port nodes, respectively. The vector $\mathbf{i}$ corresponds to the currents flowing from the nonlinear circuit part to the linear circuit part through the port nodes. Note that (4) absolutely represents the whole circuit to be analyzed because it includes the currents $\mathbf{i}$ from the nonlinear circuit part in addition to the variables and the relations of connection in the linear circuit part. Since the vector $\mathbf{i}$ is the unknown vector, however, (4) is not able to be solved alone.

Instead of solving (4), performing block matrix formulations and rewriting it lead to the following two equations

$$\mathbf{G}_{\mathrm{L11}}\mathbf{u}_{\mathrm{L}} + \mathbf{G}_{\mathrm{L12}}\mathbf{v}_{\mathrm{IF}} = \mathbf{b}_{\mathrm{L1}}, \tag{5}$$
$$\mathbf{G}_{\mathrm{L12}}^{\mathrm{T}}\mathbf{u}_{\mathrm{L}} + \mathbf{G}_{\mathrm{L22}}\mathbf{v}_{\mathrm{IF}} = \mathbf{b}_{\mathrm{L2}} + \mathbf{i}. \tag{6}$$

After the formulation process in the hierarchical technique, transforming (5) into

$$\mathbf{u}_{\mathrm{L}} = \mathbf{G}_{\mathrm{L11}}^{-1}\left(\mathbf{b}_{\mathrm{L1}} - \mathbf{G}_{\mathrm{L12}}\mathbf{v}_{\mathrm{IF}}\right) \tag{7}$$

and substituting (7) into (6) lead to

$$\mathbf{i} = \left(\mathbf{G}_{\mathrm{L22}} - \mathbf{G}_{\mathrm{L12}}^{\mathrm{T}}\mathbf{G}_{\mathrm{L11}}^{-1}\mathbf{G}_{\mathrm{L12}}\right)\mathbf{v}_{\mathrm{IF}} + \left(\mathbf{G}_{\mathrm{L12}}^{\mathrm{T}}\mathbf{G}_{\mathrm{L11}}^{-1}\mathbf{b}_{\mathrm{L1}} - \mathbf{b}_{\mathrm{L2}}\right). \tag{8}$$

Then, replacing the matrices and vectors in the equation as

$$\mathbf{A} = \mathbf{G}_{\mathrm{L22}} - \mathbf{G}_{\mathrm{L12}}^{\mathrm{T}}\mathbf{G}_{\mathrm{L11}}^{-1}\mathbf{G}_{\mathrm{L12}} \tag{9}$$
$$\mathbf{S} = \mathbf{G}_{\mathrm{L12}}^{\mathrm{T}}\mathbf{b}_{\mathrm{L11}}^{-1}\mathbf{b}_{\mathrm{L1}} - \mathbf{b}_{\mathrm{L2}} \tag{10}$$

leads to

$$\mathbf{i} = \mathbf{A}\mathbf{v}_{\mathrm{IF}} + \mathbf{S}, \tag{11}$$

where $\mathbf{A}$ denotes the port admittance matrix which describes the relations between the port node voltage $\mathbf{v}_{\mathrm{IF}}$ and the currents $\mathbf{i}$ flowing from the nonlinear circuit into the port nodes, and $\mathbf{S}$ is the current source vector which includes all current sources connected to the internal and port nodes. As a result, the linear circuit part can be regarded as the linear multi-port element of which the port admittance characteristic is defined as $\mathbf{A}$ and to which the current sources derived from $\mathbf{S}$ are connected at the port nodes as shown in Fig. 2(a). The set $(\mathbf{A}, \mathbf{S})$ is referred as the macromodel of the linear circuit part as shown in Fig. 2(b).

2.3. Formulation for Nonlinear Circuit Using Hierarchical Macromodeling

By using the macromodel $(\mathbf{A}, \mathbf{S})$ for the linear circuit part, the circuit to be analyzed can be depicted as shown in Fig. 1(b). Then, the macromodel $(\mathbf{A}, \mathbf{S})$ is stamped into the circuit equation of the whole circuit and it is written as

$$\begin{bmatrix} \mathbf{G}_{\mathrm{N11}} & \mathbf{G}_{\mathrm{N12}} \\ \mathbf{G}_{\mathrm{N12}}^{\mathrm{T}} & \mathbf{A} \end{bmatrix} \begin{bmatrix} \mathbf{u}_{\mathrm{N}} \\ \mathbf{v}_{\mathrm{IF}} \end{bmatrix} = \begin{bmatrix} \mathbf{b}_{\mathrm{N1}} \\ \mathbf{b}_{\mathrm{N2}} - \mathbf{S} \end{bmatrix}, \tag{12}$$

where $\mathbf{u}_{\mathrm{N}}$ is the voltage vector at the internal nodes in the nonlinear circuit part, $\mathbf{G}_{\mathrm{N11}}$ is the admittance matrix of the internal nodes, $\mathbf{G}_{\mathrm{N12}}$ is the admittance matrix resulting from the associations between the internal nodes and the port nodes, and $\mathbf{b}_{\mathrm{N1}}$ and $\mathbf{b}_{\mathrm{N2}}$ are the vectors of current sources connected to the internal and port nodes, respectively. Note that the port node voltage vector $\mathbf{v}_{\mathrm{IF}}$ is identical with one appearing in (4). In this formulation, it is assumed that all nonlinear circuit elements are linearized by obtaining Norton equivalents by means of the Newton-Raphson method, and therefore, different equations are formed as (12) at each Newton iteration step. We can obtain the values of the internal node voltages in the nonlinear circuit and the port node voltages at each time step by solving (12).

3. Simulation Algorithm

3.1. Simulation Algorithm for Transient Analysis

The hybrid transient analysis of linear and nonlinear circuits using the hierarchical formulation technique described in **2.2** and **2.3** is processed in the following steps.

(i) Derive the macromodel ($\mathbf{A}, \mathbf{S}$) of the linear circuit using (9) and (10).

(ii) Formulate the whole circuit by deriving the equation for the nonlinear circuit with the linear multi-port element using ($\mathbf{A}, \mathbf{S}$) and (12).

(iii) Solve the equation derived in (ii) to obtain the internal node voltages $\mathbf{u}_{\mathrm{N}}$ in the nonlinear circuit and the port node voltages $\mathbf{v}_{\mathrm{IF}}$.

(iv) Solve for the linear circuit by the fast transient analysis method such as the relaxation-based method and LIM using $\mathbf{v}_{\mathrm{IF}}$ as the input voltage from the nonlinear circuit.

These four steps are performed to obtain the all variables in the circuit at one time point, and therefore, they are iterated from (i) to (iv) until the end of the simulation. Note that because the admittance matrix $\mathbf{A}$ does not change over the iteration of a transient analysis if a fixed time step size is used, it is not needed to derive and update $\mathbf{A}$ at each step of (i). However, $\mathbf{S}$ should be updated at each time step because it includes time-varying current sources.

The procedure in the above is different from one of the hierarchical analysis in the step (iv). In [1], once the port node voltage $\mathbf{v}_{\mathrm{IF}}$ is obtained, it is substituted into (11) to calculate the current vector $\mathbf{i}$. Then, by substituting $\mathbf{i}$ into (4) and solving it using a direct method lead to the values of the internal node voltages $\mathbf{u}_{\mathrm{L}}$ in the linear circuit. Therefore, we should apply a faster transient analysis method to obtain $\mathbf{u}_{\mathrm{L}}$ compared to the direct method from the fast simulation point of view. In fact, we apply the relaxation-based method and LIM as one of the fast simulation techniques for the solution of large linear networks.

3.2. Computational Complexity of Proposed Technique

It seems that the advantage of the adoption of the direct method in (iv) is the reuse of the factored coefficient matrix: Because the factorization of the coefficient matrix is performed in the step (i) where the macromodel ($\mathbf{A}, \mathbf{S}$) is derived through the calculation of $\mathbf{G}_{\mathrm{L11}}^{-1}$, the factored matrix can be reused to solve the equation in (iv). Thus, only performing forward and backward substitutions is needed to solve (4) and the calculation amount results in $\mathcal{O}(N_{\mathrm{L}}^2)$ at each time step, where N_{L} is the number of the variables in the linear circuit. In addition, it is expected that the calculation amount is reduced if the sparsity of the matrix is effectively used.

As described above, the method which is faster than the direct method, in other words, the method of which the calculation amount is less than $\mathcal{O}(N_{\mathrm{L}}^2)$ is strongly needed in the step (iv), where the linear circuit is simulated. And therefore, the method which avoids the matrix operations such as the relaxation-based method and LIM is absolutely imperative. In fact, the calculation amount is almost linearly-increasing $\mathcal{O}(N_{\mathrm{L}}^{1\sim1.5})$ for the relaxation-based method and strictly linearly-increasing $\mathcal{O}(N_{\mathrm{L}})$ for LIM in theory. Note that even if we adopt the linearly-increasing method, we suffer from the calculation of the inverse matrix $\mathbf{G}_{\mathrm{L11}}^{-1}$ in (9) and (10) in the proposed method. However, we can reduce the costs of it by using the Cholesky factorization to derive $\mathbf{G}_{\mathrm{L11}}^{-1}$. As a result, we can deal with the large linear networks and nonlinear circuit individually without ignoring the effect between those parts by the formulation using the hierarchical technique.

4. Conclusions

In this paper, a hybrid analysis of large interconnects and nonlinear circuits using the hierarchical technique and the fast simulation technique has been described. First, we introduced the typical linear circuit formulation. Next, we described the way to derive the macromodel of the linear circuit and apply it to the hierarchical formulation of the whole circuit. Then, the simulation algorithm has been shown. Moreover, the computational complexity of the proposed technique has also been described. In conclusions, it has been confirmed that proposed technique can analyze the hybrid system adequately and more effectively than conventional ones.

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